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(54) **Hierarchic memory device**

Hierarchische Speicheranordnung

Dispositif de mémoire hiérarchique

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(73) Proprietor: **STMicroelectronics S.r.l.**
**20041 Agrate Brianza (Milano) (IT)**

(72) Inventors:
- **Pascucci, Luigi**
  **I-20099 Sesto S. Giovanni (Milano) (IT)**
- **Rolandi, Paolo**
  **I-15059 Volpedo (Alessandria) (IT)**
- **Fontana, Marco**
  **I-20100 Milano (IT)**
- **Barcella, Antonio**
  **I-24069 Trescore Balneario (Bergamo) (IT)**

(74) Representative: **Botti, Mario**
**Botti & Ferrari S.r.l.**
**Via Locatelli, 5**
**20124 Milano (IT)**

(56) References cited:
- **IEICE TRANSACTIONS, vol. E74, no. 4, 1 April 1991 pages 890-895, XP 000241311 YASUHIRO HOTTA ET AL 'A 26NS 1MBIT CMOS MASK ROM'**
- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 1B, June 1984 NEW YORK, US, pages 497-498, FITZGERALD ET AL 'Interwoven Word Lines on RAM Chips'**



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## Description

**[0001]** The present invention relates to a hierarchical memory device in accordance with the preamble of claim 1.

**[0002]** The well known architecture of a generic memory device is shown schematically in the annexed FIG. 1. It includes a storage block MX made up of a plurality of memory cells arranged in a matrix organized in rows and columns, a row decoding block RD connected at input to three address lines B0,B1,B2, a column decoding block CD connected at input to three address lines B3,B4,B5, and a read/write and possibly delete control block CNTR. The block MX is connected to the block RD through eight word-lines and to the block CD through eight bit-lines. This architecture is also described in US patent 5,193,074 at the block diagram level, the circuit level, the layout level, the silicon cross section level, and the operational level.

**[0003]** Semiconductor memory devices having architecture with hierarchical row decoding are known, e.g., again from US patent 5,193,074 at the block diagram and operational levels. The annexed FIG. 2 shows a block diagram of a simple hierarchical row decoding architecture which includes two storage sections SM each made up of a plurality of memory cells arranged in a matrix organized in rows and columns, two secondary row decoders SD and a main row decoder MD. In the diagram of FIG. 2 the decoder MD is connected at input to an address line B0 and is connected at output to two selection lines SL. The two decoders SD are connected at input both to the two lines SL and respectively to two address lines B1 and B2. The two decoders SD are also connected at output respectively to the two sections SM each through eight word lines WL.

**[0004]** There are well known reasons for using a hierarchical row decoding architecture well illustrated in the above mentioned American patent and among these are reduction of access time for equal storage capacity due to reduction of the word line length and hence resistance and reduction of the number of memory cells connected to each word line and hence their capacity.

**[0005]** The problem of reduction of word line resistance was solved in a technological manner, i.e. studying the manner and the material for making it on silicon. Normally, word lines are provided in polysilicon. A first solution for reducing the resistance is to superimpose on the polysilicon a layer of silicide. A second solution is to provide over the main word lines provided in polysilicon some auxiliary word lines provided in metallic material and to contact at regular intervals the main lines directly with the corresponding auxiliary lines.

**[0006]** These solutions are illustrated in US patent 4,827,449. In this patent there is also proposed a solution to the problem of compacting the word lines by arrangements such that the auxiliary lines would not extend for the entire length of the main lines and would not be adjacent thereto. In particular it is proposed to divide the word lines lengthwise in preferably eight sections so as to obtain uniform access time as well. But this takes place at the expense of a considerable increase in the length of the word lines since at the borders between each section and the adjacent one it is necessary to provide a space corresponding to two contacts plus the space between adjacent contacts to avoid short circuits between auxiliary word lines. In addition, the uniformity of access time is true only for cells connected to the same section and not for cells connected to different sections, especially if these sections are distant.

**[0007]** Another memory device having a hierarchical row decoding architecture is known from the document IEICE TRANSACTIONS, vol. E74, no. 4, 1 April 1991, pages 890-895, YASUHIRO HOTTA ET AL, 'A 26NS 1 MBIT CMOS MASK ROM', which represents the basis for the preamble of claim 1.

**[0008]** The purpose of the present invention is to further improve the memory devices having hierarchical row decoding architecture as concerns the duration and uniformity of access time.

**[0009]** This purpose is achieved through a memory device having the characteristics set forth in claim 1. Further advantageous embodiments of the present invention are set forth in the dependent claims.

**[0010]** By connecting the outputs of the secondary decoders, not to the end points of the word lines but to intermediate points and using auxiliary lines, access time uniformity, which is already good in the case of the hierarchical decoding, improves further.

**[0011]** In addition, if these auxiliary lines are provided in a low-resistivity material the access time is also reduced.

**[0012]** Lastly, if auxiliary lines connected to adjacent word lines are connected to adjacent secondary decoders the word lines can be compacted vertically.

**[0013]** The present invention is clarified by the description given below considered together with the annexed drawings in which

FIG. 1 shows a known architecture of a generic memory device in block diagram form,

FIG. 2 shows a known hierarchical row decoding architecture in block diagram form,

FIG. 3 shows diagrammatically part of a hierarchical row decoding architecture in accordance with the present invention,

FIG. 4 shows in layout form a first detail of the architecture of FIG. 3, and

FIG. 5 shows in layout form a second detail of the architecture of FIG. 3.

**[0014]** In the block diagram of FIG. 3 there are three secondary decoders SD each divided in a certain

number of decoding sections SDS of which only two are shown in the figure and in particular only one in detail. The complete decoding architecture corresponds to the replica of the diagram of FIG. 3 a certain number of times with the addition of a main decoder MD. More complicated decoding architectures can provide a much larger number of decoders SD, e.g. seventeen. The above mentioned US patent 5,193,074 proposes hierarchical architectures with multiple levels all usable for implementation of the present invention.

**[0015]** Among the three decoders SD are placed two storage sections SM of which the figure show only the word lines WL to which are connected the memory cells.

**[0016]** In practical production on silicon of such an architecture a section SDS must be provided in the same vertical space in which are provided two memory cells with associated two lines WL. It is thus necessary to provide an adequate horizontal space.

**[0017]** Each decoder SD is connected at input with at least one address line BL, typically different. The same line BL connects in the figure all the sections SDS of the decoder SD.

**[0018]** Each decoder SD is connected at input with at least one selection line SL, typical the same one. The same line SL connects in the figure six sections SDS of the three decoders SD. The logical signal present on the line SL is used in negated form or in normal form by the different sections SDS. This is indicated respectively as usual by the presence or absence of a small ball.

**[0019]** In FIG. 3 each section SDS has two outputs: one on the right side and one on the left side. The sections SDS belonging to decoders SD positioned near the edges of the architecture have a single output.

**[0020]** In accordance with the present invention the outputs of the decoders SD are coupled to the word lines WL through a plurality of auxiliary lines AL having first ends T1 respectively connected to the outputs and second ends T2 respectively connected to the intermediate points IT of the word lines WL. In this manner the access time to the various cells is more uniform than if the outputs of the decoders SD were connected directly to end points of the word lines WL because the signal propagation time along the word lines WL is reduced. If the points IT corresponded to the mid-points of the word lines WL the propagation time would be virtually halved.

**[0021]** If the resistivity of the auxiliary lines AL is much lower than the resistivity of the word lines WL the propagation time of the signal along the lines AL is much less than the propagation time along the word lines WL and can be ignored in a first approximation. This means that the access time is reduced on the average. If the points IT corresponded to the mid-points of the lines WL the access time would be virtually halved.

**[0022]** One way of achieving this resistivity difference consists of providing the lines WL from a layer of polysilicon preferably overlain by a layer of silicide, and in providing the lines AL from a layer of metallic material. It can be foreseen that this layer of metallic material corresponds to the layer denominated 'metal2' since the layer denominated 'metal1' is used in general for provision of the bit lines.

**[0023]** As known, the design rules call for rather large distances between adjacent structures in metallic material, for example 1.3 micron, as compared to the distances between adjacent polysilicon structures, for example 0.6 micron. To obtain good compacting of the lines AL and hence of the lines WL it is appropriate that the auxiliary lines AL connected to the adjacent word lines WL be connected to different and in particular adjacent secondary decoders SD as shown in FIG. 3. This means that lines AL connected to adjacent lines WL are not adjacent as happens to the auxiliary lines A2 and A3 connected to the word lines W2 and W3 in FIG. 5.

**[0024]** Concerning the numerical examples above mentioned the minimum width of a metallic material line is typically 1.1 micron while the minimum width of a polysilicon line is typically 0.6 micron.

**[0025]** The ideal positioning of all the intermediate points IT corresponds to the mid-point of the lines WL. In reality this is difficult to achieve because in practical production on silicon these points correspond to contacts which require rather extensive rectangular regions spaced mutually and which in general would lead to an excessive spacing of the lines WL. For this reason it is preferred to have the points IT staggered on adjacent lines WL with respect to the mid position as shown in FIG. 5 for the intermediate points I1, I2, I3, I4, I5, I6, I7, I8 respectively arranged on the lines W1, W2, W3, W4, W5, W6, W7, W8.

**[0026]** The greatest vertical compacting possible for the architecture is achieved when the auxiliary lines AL are arranged at constant distance apart corresponding to the smallest distance allowed by the design rules. In FIG. 5 this is true for the lines A1, A3, A5, A7 and the lines A2, A4, A6, A8. Naturally to achieve a smaller failure rate caused by short circuits it would be necessary to provide greater distance.

**[0027]** If because of the types of layers used to provide the lines WL and the lines AL it is not possible technologically to contact them directly, the connections between the lines WL and the lines AL are provided by means of connection structures CS provided e.g. by a different layer of metallic material as shown in FIG. 4. This is the case already discussed in which the lines WL are in polysilicon and the lines AL are in 'metal2' and in which the structures CS are in metal1. The line WL will be contacted to the structure CS by means of a path at the end T2 and the structure CS will be contacted to the lines WL by means of a 'contact' at the point IT.

**[0028]** If the vertical positioning of the lines WL is chosen on the basis of the particular cell structure used while the vertical positioning of the lines AL is chosen, regardlessly of the former, on the basis of the structure of the decoders SD and on the basis of the desired distance between adjacent lines AL, the structures CS have a different form depending on the vertical align-

ment of the line WL and the line AL which they connect. This is the case for the connection structures C1, C2, C3, C4, C5, C6, C7, C8 in FIG. 5 with respect to the corresponding word lines W1, W2, W3, W4, W5, W6, W7, W8 and the corresponding auxiliary lines A1, A2, A3, A4, A5, A6, A7, A8.

**[0029]** FIG. 5 shows in simplified layout a central portion of a storage section SM in which are displayed among other things the contacts at the intermediate points I1, I2, I3, I4, I5, I6, I7, I8.

**[0030]** As may be inferred from FIG. 5, in the vertical space of two lines WL it is possible to house two lines AL and compact the lines WL at the limit of the minimum distance furnished for the polysilicon by the design rules, on condition of having cell and decoder architectures permitting it.

**[0031]** Accordingly the solution in accordance with the present invention exhibits the great advantage of not occupying any additional space with respect to a conventional hierarchical architecture but providing an access time virtually halved and with uniformity virtually halved with respect to thereto.

**[0032]** A hierarchical row decoding architecture in accordance with the present invention can be used in a generic memory device such as that of FIG. 1.

**[0033]** Such a memory device can be provided in an integrated circuit alone or together with other circuitry such as for example a processor and constitute memory termed 'embedded'.

## Claims

1. Memory device having hierarchical row decoding architecture and comprising at least one main decoder (MD) and a plurality of secondary decoders (SD) having outputs coupled to a plurality of word lines (WL) and characterized in that said each of said word lines (WL) is connected to an output of one of said secondary decoders (SD) respectively through an auxiliary line (AL) having a first end (T1) connected to said output and a second end (T2) connected to an intermediate point (IT) of said word line (WL), the connections between each of said word lines (WL) and each of said auxiliary lines (AL) being provided by means of a connection structure (CS) provided by a layer of metallic material.

2. Device in accordance with claim 1 characterized in that the resistivity of said auxiliary lines (AL) is lower than the resistivity of said word lines (WL).

3. Device in accordance with claim 2 characterized in that said word lines (WL) are provided from a layer of polysilicon preferably overlain by a layer of silicide and in that said auxiliary lines (AL) are provided from a layer of metallic material.

4. Device in accordance with claim 1 characterized in that auxiliary lines (A2,A3) connected to adjacent word lines (W2,W3) are connected to different and in particular adjacent secondary decoders (SD).

5. Device in accordance with claim 1 characterized in that auxiliary lines (A2,A3) connected to adjacent word lines (W2,W3) are not adjacent.

6. Device in accordance with claim 1 characterized in that intermediate points (I1,I2,I3) of adjacent word lines (W1,W2,W3) are not aligned and are placed near the mid-points of said word lines (W1,W2,W3).

7. Device in accordance with claim 1 characterized in that said auxiliary lines (A1,A3,A5,A7) are arranged at a constant distance apart corresponding to the minimum distance allowed by the design rules.

8. Device in accordance with claim 1 characterized in that said structures (C1...C8) have different forms depending on the vertical alignment of the word line (WL) and auxiliary line (AL) which they connect.

9. Integrated circuit characterized in that it comprises a memory device in accordance with one of the above claims.

## Patentansprüche

1. Speichervorrichtung g mit einer hierarchischen Reihendekodierarchitektur und umfassend mindestens einen Hauptdekodierer (MD) und eine Mehrzahl von Sekundärdekodierern (SD) mit Ausgängen, die an eine Mehrzahl von Wortleitungen (WL) gekoppelt sind, dadurch gekennzeichnet, dass jede der Wortleitungen (WL) an einen Ausgang eines der Sekundärdekodierer (SD) über eine Hilfsleitung (AL) angeschlossen ist, die mit einem ersten Ende (T1) an den Ausgang und mit einem zweiten Ende (T2) an einen Zwischenpunkt (IT) der zugehörigen Wortleitung (WL) angeschlossen ist, wobei die Verbindungen zwischen den jeweiligen Wortleitungen (WL) und den zugehörigen Hilfsleitungen (AL) mit Hilfe einer Verbindungsstruktur (CS) gebildet ist, die durch eine Schicht aus metallischem Material besteht.

2. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, dass der spezifische Widerstand der Hilfsleitungen (AL) geringer ist als derjenige der Wortleitungen (WL).

3. Vorrichtung nach Anspruch 2, dadurch gekennzeichnet, dass die Wortleitungen (WL) durch eine Schicht aus Polysilizium gebildet sind, die vorzugsweise von einer Silizidschicht überlagert ist, und

dass die Hilfsleitungen (AL) durch eine Schicht aus metallischem Material gebildet sind.

4. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, dass die an benachbarte Wortleitungen (W1, W3) angeschlossenen Hilfsleitungen (A2, A3) an verschiedene und insbesondere einander benachbarte Sekundärdekodierer (SD) angeschlossen sind.

5. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, dass an einander benachbarte Wortleitungen (W2, W3) angeschlossene Hilfsleitungen (A2, A3) einander nicht benachbart sind.

6. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, dass Zwischenpunkte (I1, I2, I3) von einander benachbarten Wortleitungen (W1, W2, W3) nicht fluchten und in der Nähe der Mittelpunkte der Wortleitungen (W1, W2, W3) platziert sind.

7. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, dass die Hilfsleitungen (A1, A3, A5, A7) in konstantem Abstand voneinander angeordnet sind, welcher dem minimalen von den Entwurfsregeln zugelassenen Abstand entsprechen.

8. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, dass die Strukturen (C1,..., C8) unterschiedliche Formen aufweisen, abhängig von der vertikal Ausrichtung der Wortleitung (WL) und der Hilfsleitung (AL), die sie verbinden.

9. Integrierte Schaltung, dadurch gekennzeichnet, dass sie eine Speichervorrichtung nach einem der obigen Ansprüche aufweist.

**Revendications**

1. Dispositif de mémoire présentant une architecture de décodage hiérarchique par ligne et comprenant au moins un décodeur principal (MD) et une pluralité de décodeurs secondaires (SD) présentant des sorties couplées à une pluralité de lignes de mot (WL) et caractérisé en ce que chacune desdites lignes de mot (WL) est reliée à une sortie de l'un desdits décodeurs secondaires (SD) respectivement par l'intermédiaire d'une ligne auxiliaire (AL) présentant une première extrémité (T1) reliée à ladite sortie et une seconde extrémité (T2) reliée à un point intermédiaire (IT) de ladite ligne de mot (WL), les connexions entre chacune desdites lignes de mot (WL) et chacune desdites lignes auxiliaires (AL) étant obtenue grâce à une structure de connexion (CS) obtenue par une couche de matériau métallique.

2. Dispositif selon la revendication 1, caractérisé en ce que la résistivité des dites lignes auxiliaires (AL) est inférieure à la résistivité desdites lignes de mot (WL).

3. Dispositif selon la revendication 2, caractérisé en ce que les dites lignes de mot (WL) sont réalisées à partir d'une couche de polysilicium, de préférence recouverte d'une couche de siliciure et en ce que les dites lignes auxiliaires (AL) sont réalisées à partir d'une couche de matériau métallique.

4. Dispositif selon la revendication 1, caractérisé en ce que les lignes auxiliaires (A2, A3) reliées aux lignes de mot adjacentes (W2, W3) sont reliées à des décodeurs secondaires différents, et plus particulièrement à des décodeurs secondaires adjacents (SD).

5. Dispositif selon la revendication 1, caractérisé en ce que les lignes auxiliaires (A2, A3) reliées à des lignes de mot adjacentes (W2, W3) ne sont pas adjacentes.

6. Dispositif selon la revendication 1, caractérisé en ce que les points intermédiaires (I1, I2, I3) des lignes de mot adjacentes (W1, W2, W3) ne sont pas alignés et sont placés près de points médians des dites lignes de mot (W1, W2, W3).

7. Dispositif selon la revendication 1, caractérisé en ce que les dites lignes auxiliaires (A1, A3, A5, A7) sont placées à une distance constante correspondant à la distance minimale autorisée par les règles de construction.

8. Dispositif selon la revendication 1, caractérisé en ce que les dites structures (C1 ... C8) présentent des formes différentes selon l'alignement vertical de la ligne de mot (WL) et de la ligne auxiliaire (AL) qu'elles relient.

9. Circuit intégré, caractérisé en ce qu'il comprend un dispositif de mémoire selon l'une des revendications précédentes.

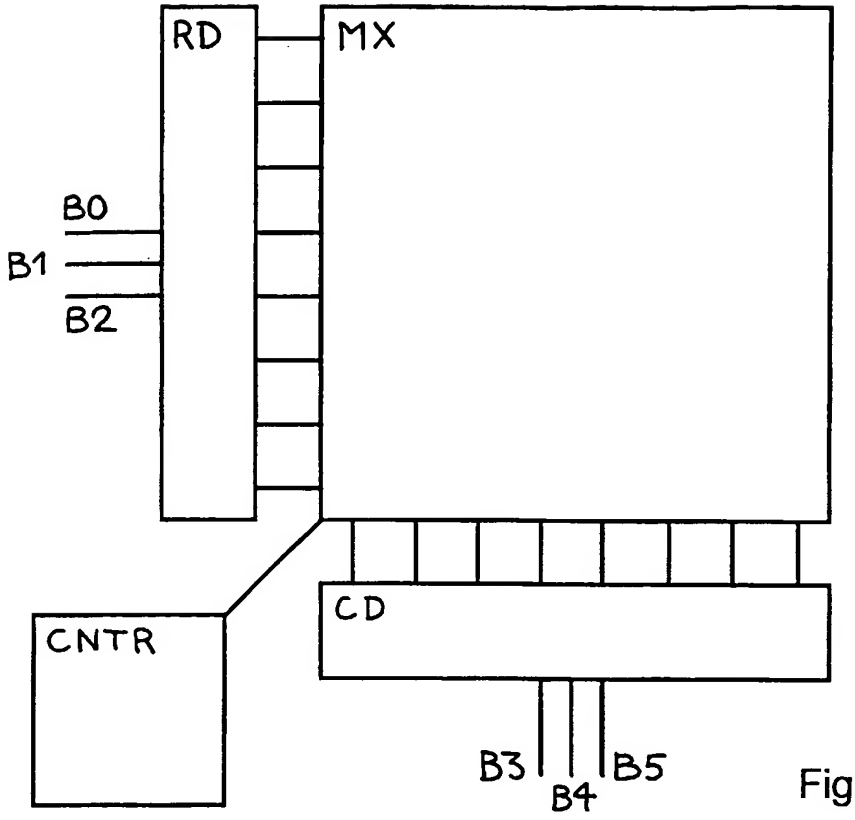


Fig.1

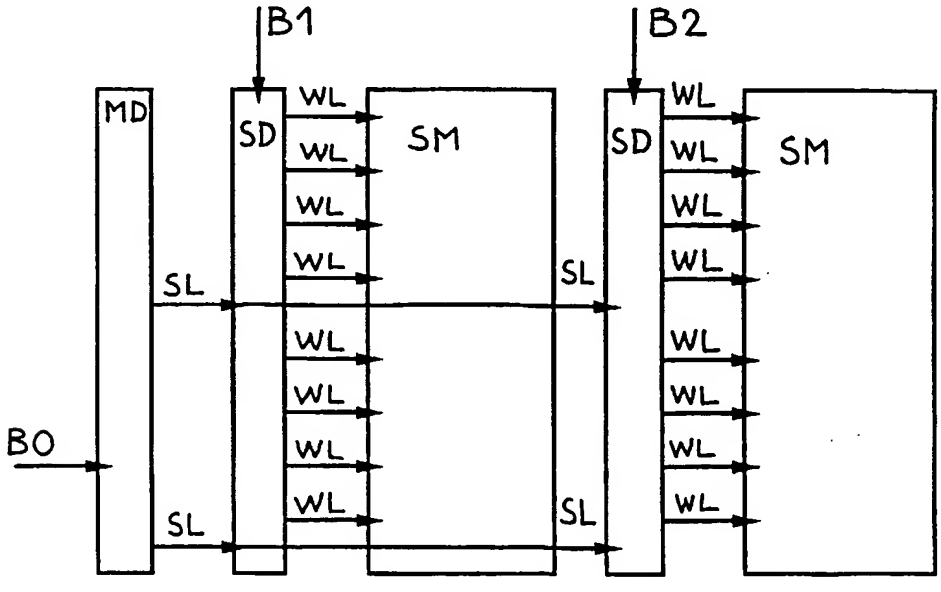


Fig.2

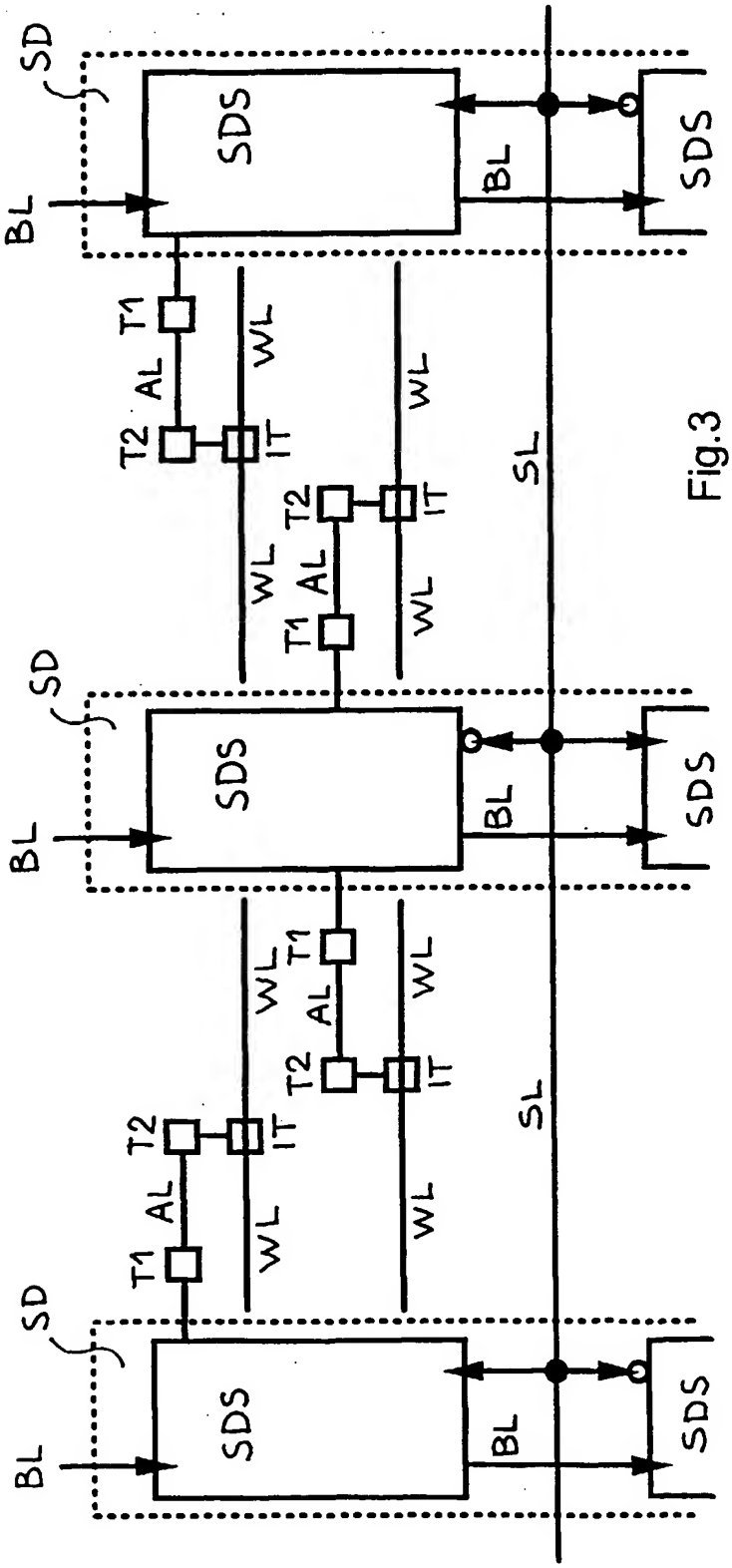
SD
SDS
BL
SDS
BL
T1
AL
T2
IT
WL
WL
SL
T2
IT
WL
AL
T1
WL
SD
SDS
BL
SDS
BL
WL
T1
AL
T2
IT
WL
T2
IT
T1
AL
WL
WL
SL
SD
SDS
BL
SDS
BL

Fig.3

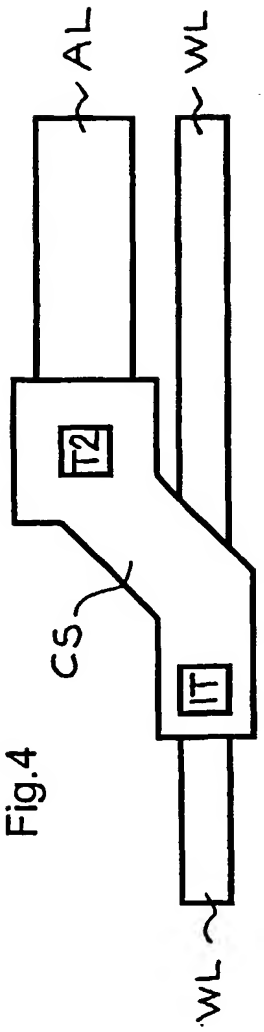
AL
WL
T2
CS
IT
WL

Fig.4

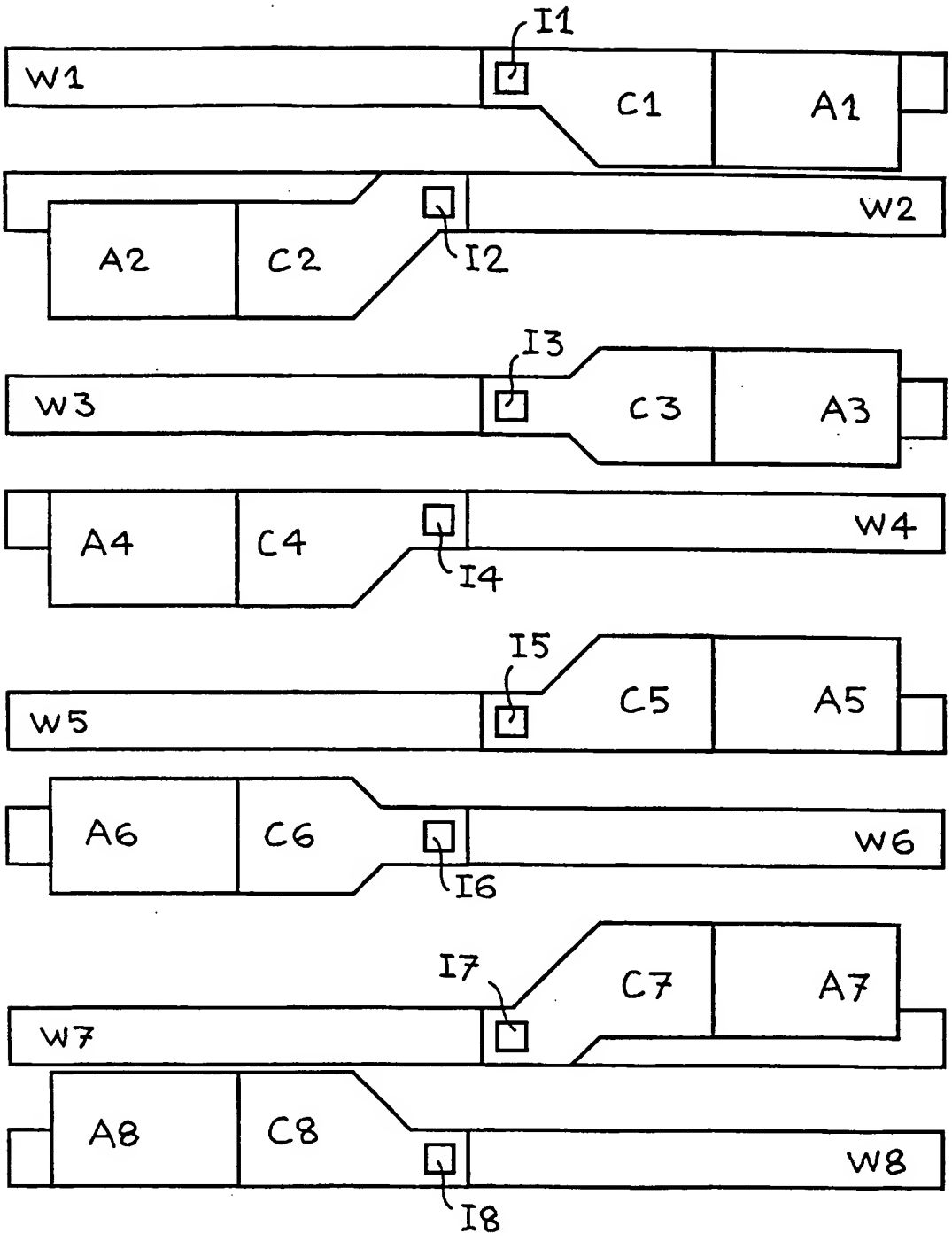
I1
W1
C1
A1
W2
A2
C2
I2
I3
W3
C3
A3
A4
C4
W4
I4
I5
W5
C5
A5
A6
C6
W6
I6
I7
C7
A7
W7
A8
C8
W8
I8

Fig.5